**Student name: Akash nag**



**Student Roll no: 2028084**



**Name of the Program: EC2093**



**Name of the Laboratory: DIGITAL ELECTRONICS LAB**



**Date: 9/9/2021**

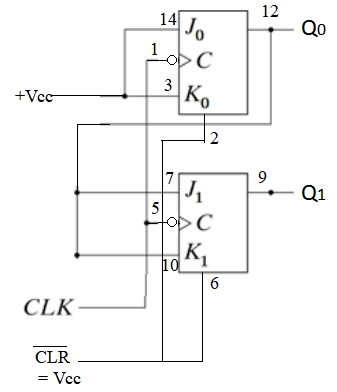
**Experiment No: 6**

***Simulation of 2-bit Synchronous Up Counter using Verilog HDL in EDA Playground.***

***Design and Verification of 2-bit Synchronous Up Counter using TinkerCAD.***

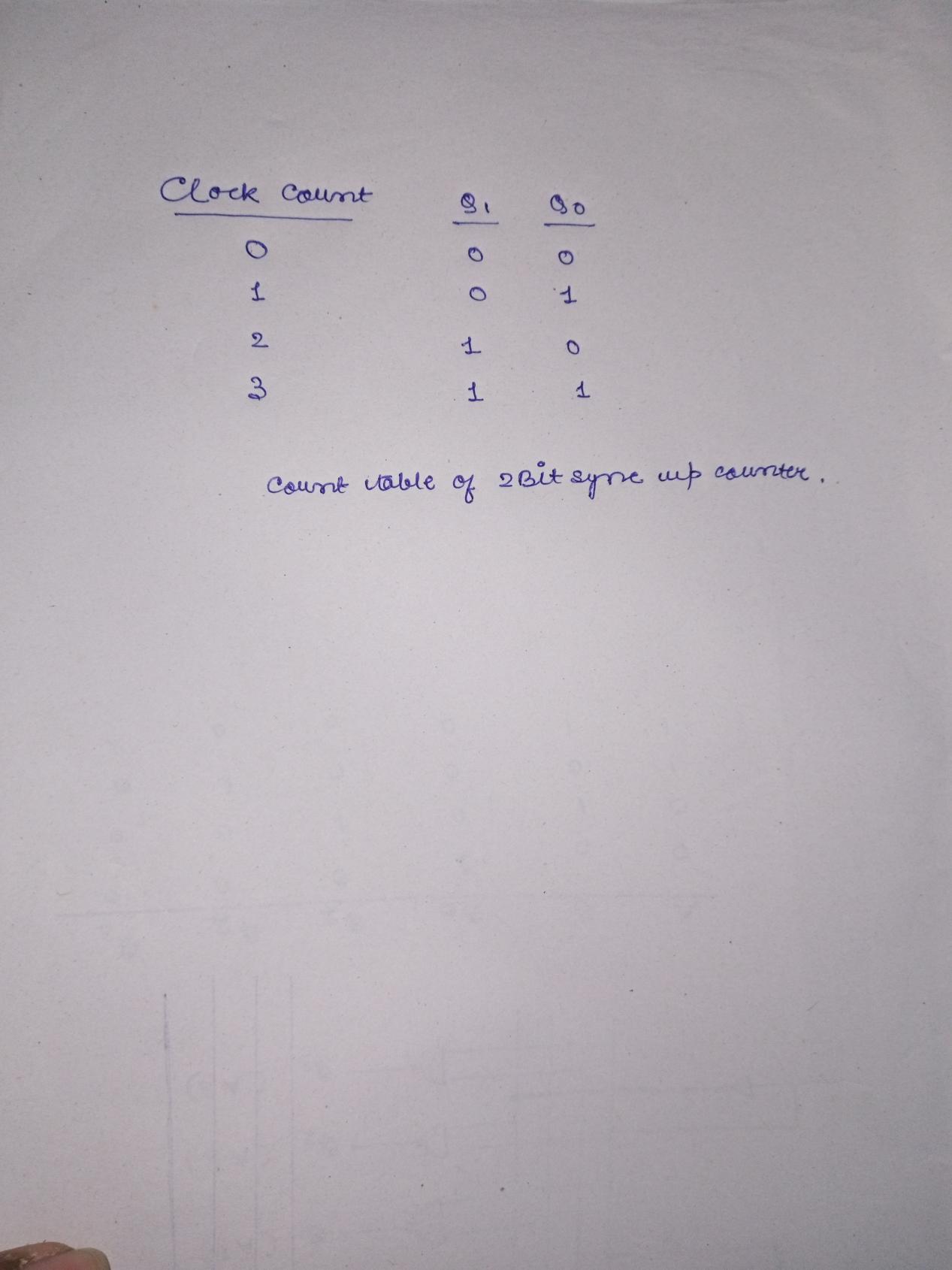
**2 bit binary synchronous up counter using J-K FF:**

**Counter:** A digital counter is a set of flip-flops (FFs) whose states change in response to pulses applied at the input to the counter. A counter can be used as a frequency divider to obtain waveforms with frequencies that are specific fractions of the clock frequency. They are also used to perform the timing function as in digital watches, to create time delays, to produce non-sequential binary counts, to generate pulse trains, and to act as frequency counters, etc. Counters may be asynchronous counters or synchronous counters. Asynchronous counters are also called ripple counters. Synchronous counters are counters in which all the FFs are triggered simultaneously (in parallel) by the clock-input pulses**.**



**Figure 1: Logic diagram of 2-bit synchronous up counter**

**Digital Logic Diagram and Truth Table :**

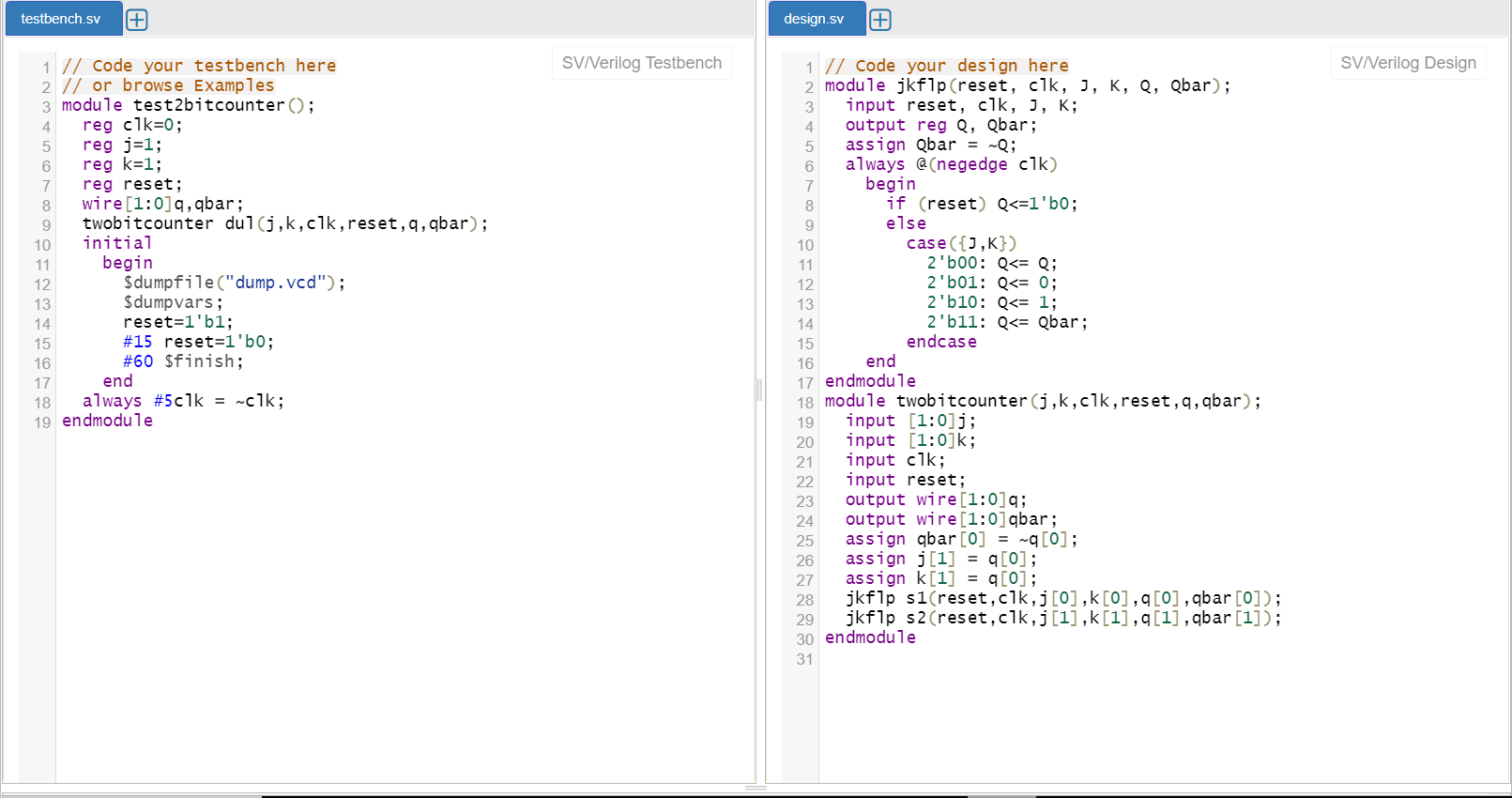
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**Components required***:*

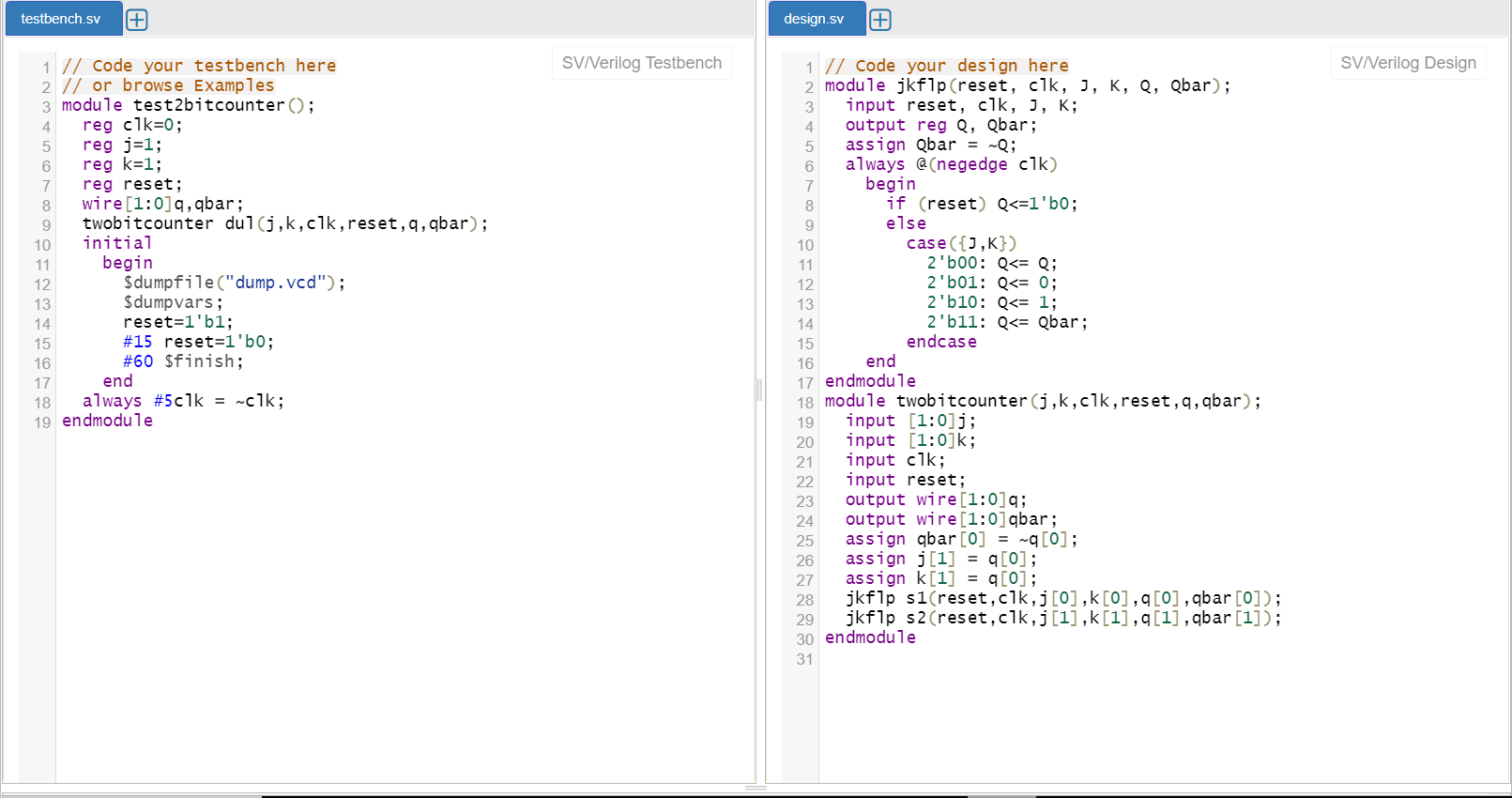
1. ICs- 7473
2. Bread board
3. Power supply
4. LED
5. Resistor(220 ohm)
6. Sliding switches
7. Connecting wires

**Simulation platform:**  *EDA playground and TinkerCAD*

**Verilog HDL Code:**



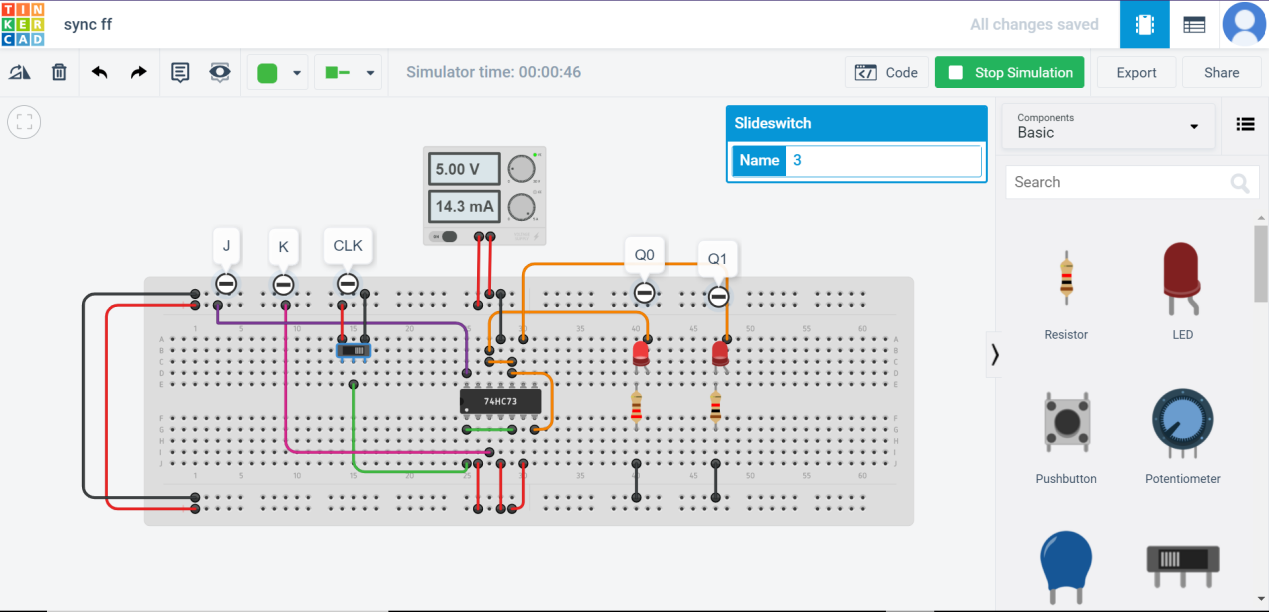
**Test bench code:**

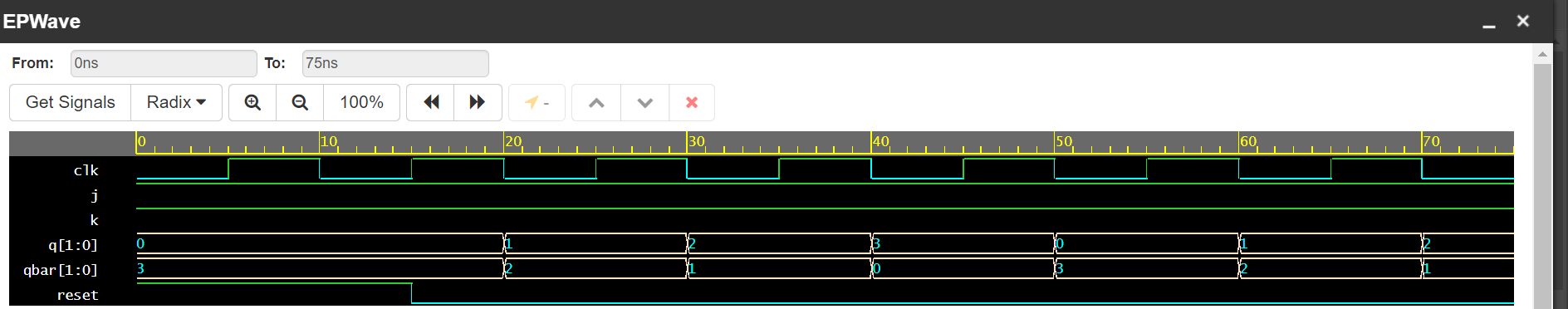


**Web Link to the EDA playground file saved by the student in his account:**

<https://www.edaplayground.com/x/QyHc>

**Observations:**

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|  |  |  |
| --- | --- | --- |
| CLK Count | Q1 | Q0 |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 1 | 0 |
| 3 | 1 | 1 |

By seeing the waveform, we can infer that the state of the flipflop changes in response to the pulses applied in the counter. The number of clock count applied is depicted by the glowing of the LEDs. Similar is seen in case of the EPA graph.

**Conclusion:** By performing the experiments on tinkercad and eda playground , the functioning of the 2 bit binary synchronous up counter using J-K FF along with the truth table is verified.

**Student Full name & Roll no:**

